two pairs of linear feedback shift registers, wherein second seed values for the second pair of linear feedback shift registers are different from first seed values for the first pair of linear feedback shift registers, the second seed values being calculated from the first seed values, wherein the first and second pair of linear feedback shift registers are implemented to produce more than one new state bit and more than one output bit for each linear feedback shift registers at the same time.

2. (Original) The gold code generator of claim 1 wherein the seed values for the second pair of linear feedback shift registers are delayed values of the first seed values.

3. (Previously amended) The gold code generator of claim 1 wherein the gold code generator is implemented on a reconfigurable ~~logic~~ chip.

4. (Original) The gold code generator of claim 3 wherein the calculation of some of the second seed values is done using a dedicated processor on the reconfigurable chip.

5. (Original) The gold code generator of claim 3 wherein the gold code generator configuration is loaded into a background plane of the reconfigurable chip, while the reconfigurable chip is operating on another configuration in the foreground.

6. (Original) The gold code generator of claim 3 wherein the feedback is implemented using lookup tables.

7-11. (previously canceled).

12. (Original) A method of implementing a pseudo-random code generator:

converting a psuedo-random code generator specification into an equivalent representation, the psuedo-random code generator specification being such that taps used to calculate an output include at least one tap within n spaces from the input, the equivalent representation is such that no such taps are within n spaces from the input; and

implementing the equivalent representation such that multiple new state bits are calculated at the same time.

13. (Currently Amended) The method of claim 12 wherein the pseudo-random code generator specification being such that taps to calculate an output is defined within a first ~~chip~~ shift register span, the equivalent representation is such that taps to calculate an output bit are within a smaller shift register span.

14. (Original) The method of claim 12 wherein the equivalent representation includes two pairs of linear feedback shift registers wherein the second seed values for the second pair of linear feedback shift registers is different from a first seed value for the first pair of linear feedback shift registers.

15. (Original) The method of claim 12 wherein the pseudo-random code generator comprises a gold code generator.

16. (Original) The method of claim 12 wherein the pseudo-random code generator is implemented on a reconfigurable chip.

17. (Original) A method of implementing a pseudo-random code generator comprising:

converting a pseudo-random code generator specification into an equivalent representation, the psuedo-random code generator specification being such that taps to calculate an output are defined within a first shift register span, the equivalent representation is such that the taps to calculate an output bit are within a smaller shift register span; and

implementing the equivalent representation such that multiple output bits are calculated at the same time.

18. (Original) The method of claim 17 wherein the pseudo-random code generation specification is such that taps used to calculate an output have at least one tap within *n* spaces from the input, the equivalent representation is such that no such tap is within *n* spaces from the input.

19. (Original) The method of claim 17 wherein two pairs of linear feedback shift registers are used in the equivalent representation.

20. (Original) The method of claim 19 wherein the second seed values for the second pair of linear feedback shift registers are different from the first seed values for the first pair of linear feedback shift registers.

21. (Original) The method of claim 17 implemented on a reconfigurable chip.

22. (Original) The method of claim 17 wherein in the equivalent representation of the output bits are calculated from taps at a single register for each linear feedback shift register.

23. (Previously Added) A system comprising:

a gold code generator, wherein the gold code generator comprises multiple pairs of linear feedback shift registers implemented to simultaneously produce more than one state bit and more than one output bit for each linear feedback shift registers;

at least one reconfigurable chip where reconfigurable elements are selectively configured by at least the output of the gold code generator; and

a communication element, coupled with the reconfigurable chip, to receive output from the at least one reconfigurable chip to enable wireless communication.

24. (Previously Added) The system of claim 23 wherein the gold code generator configuration is loaded into a background plane of the at least one reconfigurable chip, while the at least one reconfigurable chip is operating on another configuration in a foreground plane, wherein once the gold code generator is loaded into the background plane, the gold code generator configuration can be activated to produce an output, at least a subset of which is used to reconfigure the at least one reconfigurable chip.

25. (Previously Added) The system of claim 24 wherein the configuration in the foreground plane

is an other gold code generator configuration.

26. (Previously Added) The system of claim 23 wherein a seed value for a first pair of linear feedback shift registers are different from a seed value for other pairs of linear feedback shift registers.

27. (Previously Added) The system of claim 26 wherein a subsequent seed value is calculated from the first seed value.

28. (Previously Added) The system of claim 27 wherein the calculation of the subsequent seed value is done at least partially in a processor on the at least one reconfigurable chip.

29. (Previously Added) The system of claim 23 wherein the gold code generator is implemented on an at least one reconfigurable chip.

30. (Previously Added) The system of claim 23 wherein the communication element is a transmitter for spread spectrum transmission.

31. (Previously Added) The system of claim 23 wherein the communication element is a receiver for spread spectrum reception.

32. (Previously Added) A gold code generator comprising:

multiple pairs of linear feedback shift registers to simultaneously produce more than one state bit and more than one output bit for each pair of linear feedback shift registers.

33. (Previously Added) The gold code generator of claim 32 wherein the gold code generator is implemented on a reconfigurable chip.

34. (Previously Added) The gold code generator of claim 33 wherein the gold code generator configuration is loaded into a background plane of the reconfigurable chip, while the reconfigurable chip is operating on another configuration in a foreground plane.

35. (Previously Added) The gold code generator of claim 33 wherein feedback is implemented using lookup tables.

36. (Previously Added) The gold code generator of claim 32 wherein a seed value for the gold code generator for a first pair of linear feedback shift registers are different from a seed value for other pairs of linear feedback shift registers.

37. (Previously Added) The gold code generator of claim 36 wherein the seed value for the other pairs of linear feedback shift registers is calculated from the first seed value.

38. (Previously Added) The gold code generator of claim 36 wherein the calculation of the seed value for the other pairs of linear feedback shift registers is done at least partially in a processor on the reconfigurable chip.